Claims

What is claimed is:

1. A dual mode, analog differential and complementary metal oxide semiconductor (CMOS) logic circuit comprising:

a differential input for receiving a differential input signal;

a switch pair coupled to said differential input;

a pair of load resistors coupled to said switch pair defining a differential output for providing a differential output signal;

a current source coupled to said switch pair;

a control input for receiving a control signal; and

control circuitry coupled to said control input for disabling said current source to select a CMOS testing mode responsive to said control signal being activated.

2. A dual mode, analog differential and complementary metal oxide semiconductor (CMOS) logic circuit as recited in claim 1 includes a first pair of field effect transistors and a second pair of field effect transistors connected in parallel between said pair of load resistors and a voltage supply rail; said first pair of field effect transistors being substantially larger than said second pair of field effect transistors.

3. A dual mode, analog differential and complementary metal oxide semiconductor (CMOS) logic circuit as recited in claim 2 wherein said first pair of field effect transistors connect said pair of load resistors to said voltage supply rail during normal analog differential mode and being open during the CMOS logic mode responsive to said control signal being activated.

4. A dual mode, analog differential and complementary metal oxide semiconductor (CMOS) logic circuit as recited in claim 3 wherein said second pair of field effect transistors connect said pair of load resistors to said voltage supply rail during the CMOS testing mode.

5. A dual mode, analog differential and complementary metal oxide semiconductor (CMOS) logic circuit as recited in claim 2 wherein said first pair of field effect transistors and said first pair of field effect transistors are P-channel FETs (PFETs).

6. A dual mode, analog differential and complementary metal oxide semiconductor (CMOS) logic circuit as recited in claim 5 wherein said control signal is applied to a gate input of said first pair of field effect transistors.

7. A dual mode, analog differential and complementary metal oxide semiconductor (CMOS) logic circuit as recited in claim 5 wherein said switch pair are a switch pair of N-channel field effect transistors (NFETs).

8. A dual mode, analog differential and complementary metal oxide semiconductor (CMOS) logic circuit as recited in claim 6 wherein said second pair of PFETs and said switch pair of NFETs form a pair of CMOS inverters during the CMOS testing mode.

9. A dual mode, analog differential and complementary metal oxide semiconductor (CMOS) logic circuit as recited in claim 8 wherein said pair of CMOS inverters during the CMOS testing mode provide said differential output signal of a full rail-to-rail swing signal.

10. A dual mode, analog differential and complementary metal oxide semiconductor (CMOS) logic circuit as recited in claim 7 wherein said current source is an NFET current source connected between a common source node connection of said NFET switch pair and ground and a bias input signal is applied to a gate of said NFET current source.

11. A dual mode, analog differential and complementary metal oxide semiconductor (CMOS) logic circuit as recited in claim 10 wherein said control circuitry includes a control NFET connected in parallel with said NFET current source and said control signal is applied to a gate of said control NFET.

12. A dual mode, analog differential and complementary metal oxide semiconductor (CMOS) logic circuit as recited in claim 1 wherein a differential clock buffer circuit is formed by a first stage and a second stage of the dual mode, analog differential and CMOS logic circuit connected in series.

13. A dual mode, analog differential and complementary metal oxide semiconductor (CMOS) logic circuit as recited in claim 1 wherein a differential multiplexer circuit includes an output stage formed by the dual mode, analog differential and CMOS logic circuit.

14. A dual mode, analog differential and complementary metal oxide semiconductor (CMOS) logic circuit as recited in claim 1 wherein a differential latch circuit includes an output stage formed by the dual mode, analog differential and CMOS logic circuit.

15. A dual mode, analog differential and complementary metal oxide semiconductor (CMOS) logic circuit as recited in claim 1 wherein said current source is an NFET current source and a bias input signal is applied to a gate of said NFET current source via a resistor capacitor filter circuit.

16. A dual mode, analog differential and complementary metal oxide semiconductor (CMOS) logic circuit comprising:

a differential input for receiving a differential input signal;

a switch pair of field effect transistors coupled to said differential input;

a pair of load resistors coupled to said switch pair of field effect transistors defining a differential output for providing a differential output signal;

a first pair of field effect transistors and a second pair of field effect transistors connected in parallel between said pair of load resistors and a voltage supply rail; said first pair of field effect transistors being substantially larger than said second pair of field effect transistors;

a current source field effect transistor coupled to said switch pair of field effect transistors;

a control input for receiving a control signal; and

control circuitry coupled to said control input for disabling said current source to select a CMOS testing mode responsive to said control signal being activated.

17. A dual mode, analog differential and complementary metal oxide semiconductor (CMOS) logic circuit as recited in claim 1 wherein said first pair of field effect transistors and said first pair of field effect transistors are P-channel FETs (PFETs); and said switch pair of field effect transistors are N-channel field effect transistors (NFETs).

18. A dual mode, analog differential and complementary metal oxide semiconductor (CMOS) logic circuit as recited in claim 17 wherein said first pair of PFETs connect said pair of load resistors to said voltage supply rail during normal analog differential mode and are open during the CMOS testing mode responsive to said control signal being activated.

19. A dual mode, analog differential and complementary metal oxide semiconductor (CMOS) logic circuit as recited in claim 17 wherein said second pair of PFETs connect said pair of load resistors to said voltage supply rail during the CMOS testing mode.

20. A dual mode, analog differential and complementary metal oxide semiconductor (CMOS) logic circuit as recited in claim 17 wherein said second pair of PFETs and said switch pair of NFETs form a pair of CMOS inverters during the CMOS testing mode.